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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,919	02/17/2004	Tingkai Li	SLA0772	1905

27518 7590 07/28/2008

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EXAMINER	
TALBOT, BRIAN K	

ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
07/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,919	LI ET AL.	
	Examiner	Art Unit	
	Brian K. Talbot	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 8* is/are allowed.

6)☒ Claim(s) *5,7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The response filed 4/1/08 has been considered and entered. Claims 1-4 and 13-19 have been canceled. Claims 5-12 remain in the application.

2. In light of the Terminal Disclaimer filed 4/1/08 and approved on 5/28/08, the Double Patenting Rejection has been withdrawn.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37

CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

6. Claims 5,7 and 9-12 are rejected under 35 U.S.C. 103(a) as being obvious over Yano et al. (6,387,712) or Park (5,524,092) in combination with either Asano et al. (6,407,422), Li et al. (6,483,137) or Li et al. (6,475,813) further in combination with IBM Technical Disclosure Bulletin, March 1977.

Yano et al. (6,387,712) teaches a process for preparing ferroelectric films. A silicon substrate is coated with conductive subbing layer and then with a ferroelectric layer. The conductive subbing layer functions as an electrode and includes indium-containing oxides (col. 10, line 65 – col. 35). Yano et al. (6,387,712) teaches a silicon substrate with a silicon oxide layer formed thereon (col. 17, lines 53-60 and col. 20, line 20 – col. 21, line 25).

Park (5,524,092) teaches a multilayered ferroelectric semiconductor device whereby an indium tin oxide layer is applied followed by a ferroelectric film (col. 4, lines 11-65).

Yano et al. (6,387,712) or Park (5,524,092) fail to teach forming the ferroelectric film by a MOCVD process.

Asano et al. (6,407,422) teaches a memory device whereby a silicon substrate (11) has a layer of metal (51) including indium/indium oxide deposited thereon. An oxide layer (52) is applied to the layer (51). Patterning and selective etching of the layer indium/indium oxide layer (51) is performed. Deposition of a ferroelectric material and top electrode are formed to complete the device. The ferroelectric layer is applied by MOCVD (col. 1, lines 15-25 and col. 5, lines 45-60).

Li et al. (6,483,137) teaches the claimed processing parameters for forming the PGO film by MOCVD with an injector and precursor gases (abstract and col. 2, line 60 – col. 8, line 45).

Li et al. (6,475,813) teaches the claimed processing parameters for forming the PGO film by MOCVD with an injector and precursor gases (abstract and col. 2, line 25 – col. 3, line 50).

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified Yano et al. (6,387,712) or Park (5,524,092) process by forming the PGO film by MOCVD as detailed by Asano et al. (6,407,422), Li et al. (6,483,137) or Li et al. (6,475,813) with the expectation of achieving similar results.

Yano et al. (6,387,712) or Park (5,524,092) in combination with either Asano et al. (6,407,422), Li et al. (6,483,137) or Li et al. (6,475,813) fail to teach a buffered HF treatment prior to forming the indium oxide.

IBM Technical Disclosure Bulletin, March 1977 teaches cleaning a silicon substrate with buffered HF prior to coating thereon.

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified Yano et al. (6,387,712) or Park (5,524,092) in combination with either Asano et al. (6,407,422), Li et al. (6,483,137) or Li et al. (6,475,813) to include a cleaning step with buffered HF as evidenced by IBM Technical Disclosure Bulletin, March 1977 with the advantage of preparing the silicon substrate for subsequent deposition thereon with improved adhesion between the coating and substrate resulting from the "clean" substrate.

Regarding claim 7, the Examiner recognizes that the prior art fails to teach the claimed processing parameters for forming the In2O3 film.

While the Examiner acknowledges this fact, it is the Examiner's position that sputtering indium oxide films are conventional in the art and the processing parameters utilized to produce the indium oxide film would be a matter of design choice of one practicing in the art dependent upon the desired final product. Absence a showing of unexpected results garnered from the specific claimed parameters, it is the Examiner's position that one skilled in the art would have had a reasonable expectation of success optimizing these well known processing parameters.

Allowable Subject Matter

7. Claims 6 and 8 are allowed.

Reasons for Allowance

8. The following is an examiner's statement of reasons for allowance:

The prior art fails to teach the claimed invention including a high-k layer between the silicon substrate and the indium oxide layer followed by a ferroelectric material formed by MOCVD .

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Amendment

9. Applicant's arguments with respect to claims 5,7 and 9-12 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that the prior art fails to teach treating the silicon substrate with a buffered HF solution prior to forming the indium oxide layer.

IBM Technical Disclosure Bulletin, March 1977 teaches cleaning a silicon substrate with buffered HF prior to coating thereon.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian K. Talbot whose telephone number is (571) 272-1428. The examiner can normally be reached on Monday-Friday 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian K Talbot/
Primary Examiner, Art Unit 1792

BKT